AUTOMATIC TIMING ANALYZER

ABSTRACT OF THE DISCLOSURE

A test methodology is used to conduct an automatic chip timing

analysis in coarse and fine resolution steps. Timing adjustment circuits

5   implement coarse timing adjustment and fine timing adjustment for chip

timing analysis. Timings such as clock, address and control inputs to a

memory system can be digitally adjusted with respect to each other. A timer

circuit is provided with a counter so that an incremental or decremental timing

analysis can be carried out with a specific timing step. An algorithm is

10   implemented which provides an effective, low-cost and accurate timing

analysis. A nested loop is set up in the BIST where all possibilities of timing

relationships between two or more signals can be applied to a device under

test, and weaknesses, or failing timing conditions, can be found.

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